

PTO/SB/08A (09-06)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known	
	Application Number	10/761,156
	Filing Date	January 20, 2004
	First Named Inventor	Stephen Paul Wilcox
	Art Unit	2825
	Examiner Name	L. Garbowski
Sheet 1 of 2	Attorney Docket Number	104969-50921 (302715)

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
M		US- 5,502,648	03-1996	Kaplan, Jonathan T.	
W		US- 6,874,134	03-2005	Collin et al.	
W		US- 6,252,448	06-2001	Schober, Robert C.	
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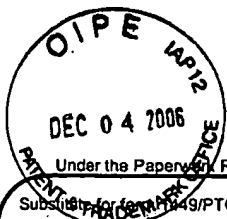
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	MM-DD-YYYY			

Examiner Signature		Date Considered	12/8/6
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Sheet	2	of	2	Attorney Docket Number	104969-50921 (302715)

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
W		Wu et al., Clock-gating and Its Application to Low Power Design of Sequential Circuits, March 2000, IEEE, Vol. 47, Pages 415-419.	
W		Lang et al., Individual Flip Flop with Gated Clocks for Low Power Datapaths, June 1997, IEEE, Vol. 44, Pages 507-516.	

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